A formal study of two physical countermeasures against side channel attacks

PROOFS'2012

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Physical Attacks

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Extra logic is required in order to mask the sensitive data or to balance the leakage.

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empty circuit

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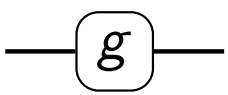

logical gate $g \in \mathcal{G}$

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a single wire

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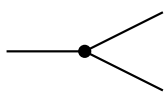

a fork

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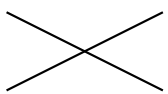

a swap

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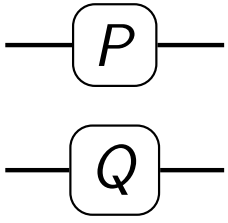

parallel composition

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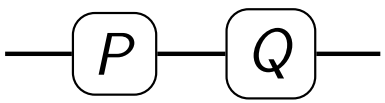

sequential composition

Well-formedness

Circuit with n inputs and m outputs

$$\frac{\mathcal{T}(g) = (n, m)}{g : n \otimes m}\ g \in \mathcal{G}$$

$$\frac{}{\mathbf{0} : 0 \otimes 0} \qquad \frac{}{\mathbf{I} : 1 \otimes 1} \qquad \frac{}{\mathbf{Y} : 1 \otimes 2} \qquad \frac{}{\mathbf{X} : 2 \otimes 2}$$

$$\frac{P_1 : n_1 \otimes m_1 \qquad P_2 : n_2 \otimes m_2}{P_1 \parallel P_2 : n_1 + n_2 \otimes m_1 + m_2} \qquad \frac{P_1 : n \otimes m \qquad P_2 : m \otimes p}{P_1 \,;\, P_2 : n \otimes p}$$

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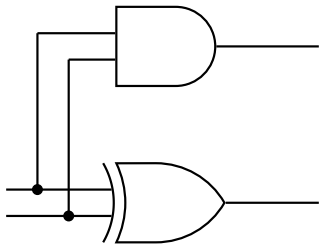
Example: a half-adder

$$\mathcal{G} = \{\mathrm{AND}, \mathrm{XOR}\}$$



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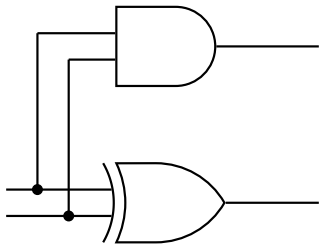

$$\mathsf{Half} := (\mathbf{Y} \,\|\, \mathbf{Y})\,;\, (\mathbf{I} \,\|\, \mathbf{X} \,\|\, \mathbf{I})\,;\, (\mathrm{AND} \,\|\, \mathrm{XOR})$$

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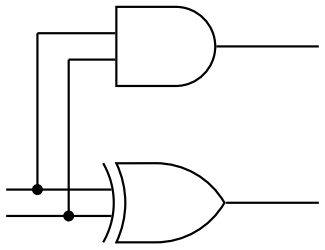

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Half is a combinational circuit with 2 inputs and 2 outputs, i.e. $\mathsf{Half} : 2 \otimes 2$.

Preliminary definitions

Alphabet, words, concatenation.

An alphabet Σ is a finite set of letters.
A word u over Σ is a finite sequence of letters $u = u_1 \cdots u_n$ where $u_i \in \Sigma$.
The set of words over Σ is noted Σ^*.
The integer n is the length of u and noted $|u|$.
The empty word is noted ϵ and is the unique word of length 0.
The set of words of length n is noted Σ^n.
The concatenation of $u = u_1 \cdots u_n$ and $v = v_1 \cdots v_m$ is defined $u \bullet v := u_1 \cdots u_n v_1 \cdots v_m$.

Formal semantics

C computes y on input x

The semantics of circuits is given by a relation of $\Sigma^* \times \Sigma^*$.

$$\frac{x \in \Sigma^* \qquad \mathcal{E}(g)(x) = y \in \Sigma^*}{g \Vdash x \rightsquigarrow y}\ g \in \mathcal{G} \qquad \frac{}{\mathbf{0} \Vdash \epsilon \rightsquigarrow \epsilon}$$

$$\frac{}{\mathbf{I} \Vdash a \rightsquigarrow a}\ a \in \Sigma \qquad \frac{}{\mathbf{Y} \Vdash a \rightsquigarrow aa}\ a \in \Sigma \qquad \frac{}{\mathbf{X} \Vdash ab \rightsquigarrow ba}\ a, b \in \Sigma$$

$$\frac{P_1 \Vdash x_1 \rightsquigarrow y_1 \qquad P_2 \Vdash x_2 \rightsquigarrow y_2}{P_1 \parallel P_2 \Vdash x_1 \bullet x_2 \rightsquigarrow y_1 \bullet y_2} \qquad \frac{P_1 \Vdash x \rightsquigarrow y \qquad P_2 \Vdash y \rightsquigarrow z}{P_1 \,;\, P_2 \Vdash x \rightsquigarrow z}$$

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$\mathcal{E}(g)$ is a partial function $\Sigma^* \rightharpoonup \Sigma^*$, defined consistently w.r.t. the typing function.

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$$P \simeq Q \iff \forall x, y : P \Vdash x \rightsquigarrow y \iff Q \Vdash x \rightsquigarrow y$$

Structural congruence

$\equiv$ identifies circuits that only differ in some minor wiring details.

It is the smallest congruence that satisfies the following equations:

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- If $P_1 : n \otimes m$ and $P_2 : m \otimes p$ then
  $(P_1 \,;\, P_2) \| (P_3 \,;\, P_4) \equiv (P_1 \| P_3) \,;\, (P_2 \| P_4)$

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Some results

- If $P : n \otimes m$ and $P : n' \otimes m'$ then $n = n'$ and $m = m'$.
- If $P \equiv Q$ then $P : n \otimes m \iff Q : n \otimes m$.
- If $P \Vdash x \rightsquigarrow y$ then $P : |x| \otimes |y|$.
- If $P : n \otimes m$ and $P \Vdash x \rightsquigarrow y$ then $|x| = n$ and $|y| = m$.
- If $P : n \otimes m$ then for any x such that $|x| = n$ there exists y such that $P \Vdash x \rightsquigarrow y$.
- If $P \Vdash x \rightsquigarrow y$ and $P \Vdash x \rightsquigarrow z$ then $y = z$.
- $\simeq$ is a congruence.
- If P and Q are ill-formed then $P \simeq Q$.
- $\equiv \subseteq \simeq$.

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Definitions

- In the following, let $\Sigma = \{0, 1\}$.
- We pose $T = 10$, $F = 01$, $N = 00$ et $E = 11$.
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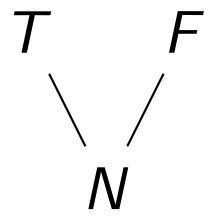

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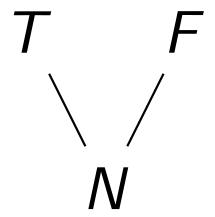

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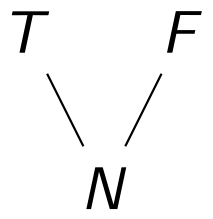
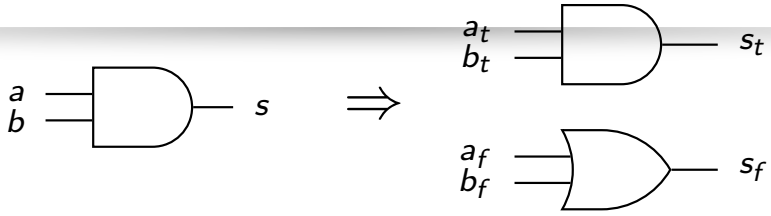


- Let $\sim$ be the equivalence relation on Σ^2 whose equivalence classes are NULL, VALID and FAULT.
- We extend these definitions to words of even length.
- For $u \in \Sigma^*$, we let $[u] \in \mathrm{VALID}^*$ be the corresponding word in dual-rail logic.
  example: $[0110] = FTTF = 01101001$

Transformation process



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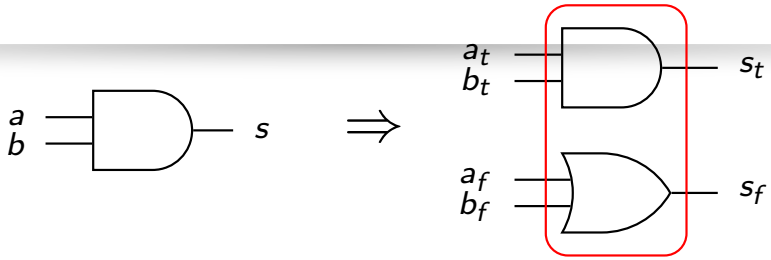

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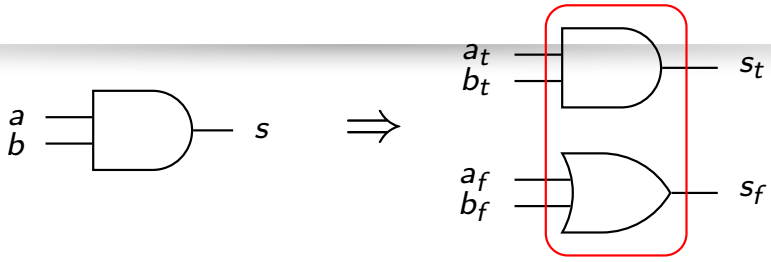

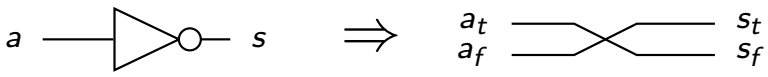

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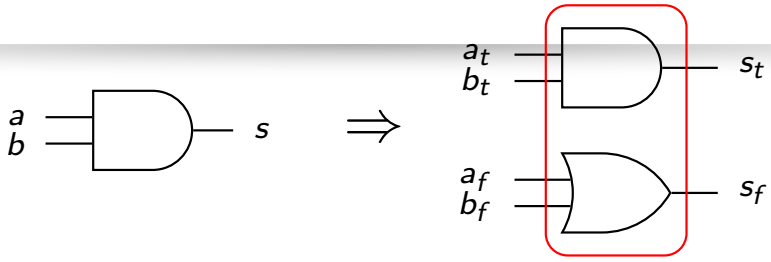

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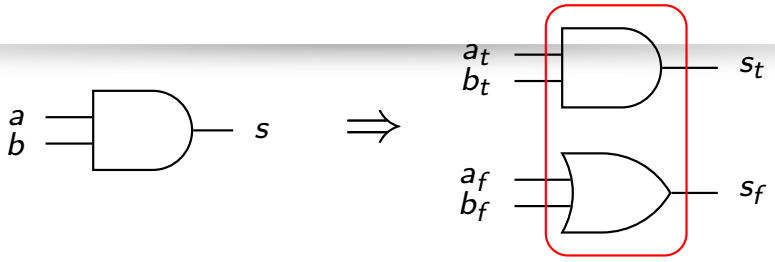

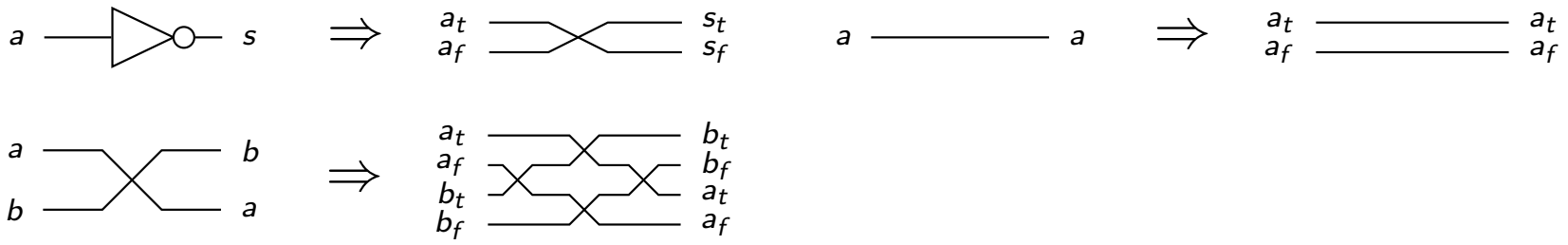

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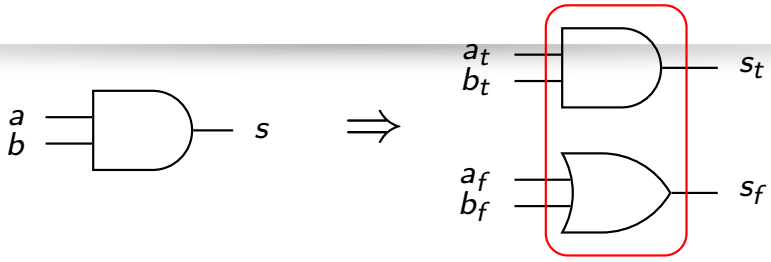

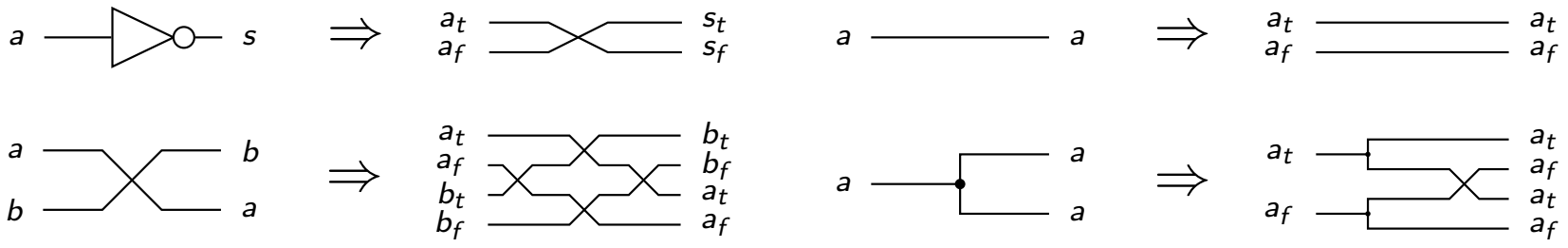

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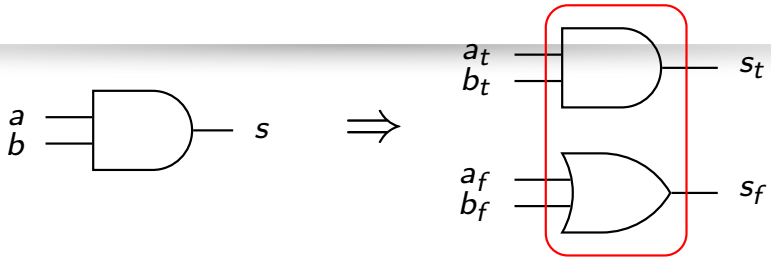
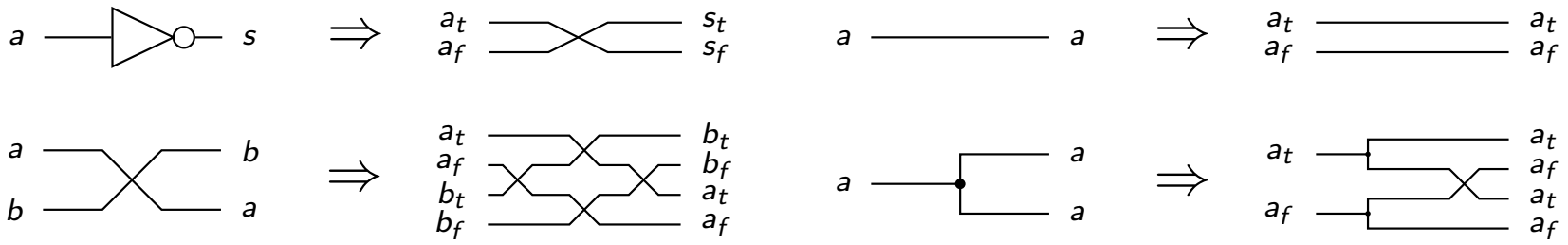
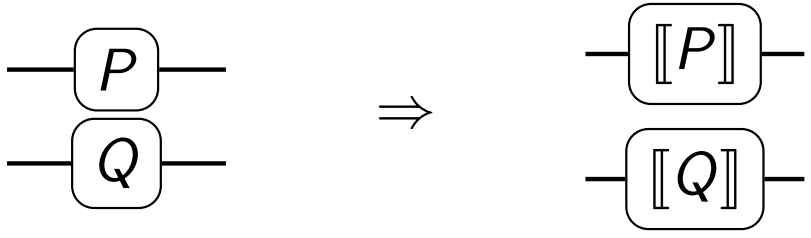
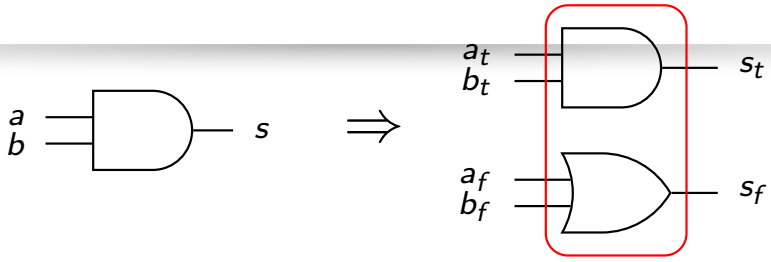
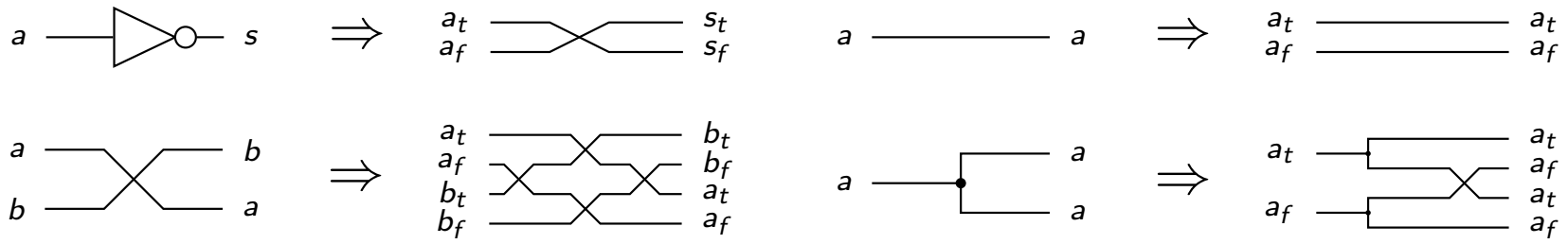


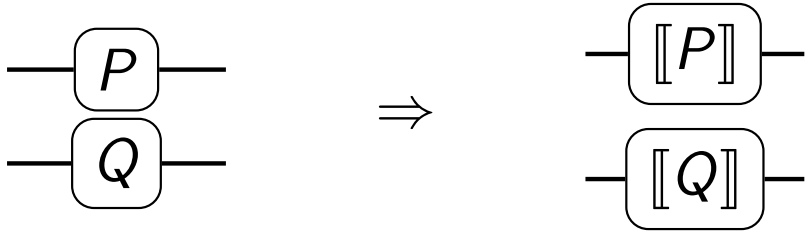


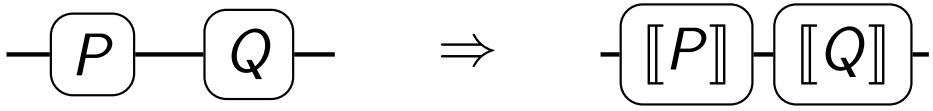


Transformation process









Properties

$[\![P]\!]$ fulfils the DPL invariants.

- If $[\![P]\!] \Vdash x \rightsquigarrow y$ and $x \in \mathrm{NULL}^*$ then $y \in \mathrm{NULL}^*$.
- If $[\![P]\!] \Vdash x \rightsquigarrow y$ and $x \in \mathrm{VALID}^*$ then $y \in \mathrm{VALID}^*$.

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The transformation is sound.

If $P \Vdash x \rightsquigarrow y$ then $[\![P]\!] \Vdash [x] \rightsquigarrow [y]$.

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No glitches are possible.

$$[\![P]\!] \Vdash x \rightsquigarrow y$$

Properties

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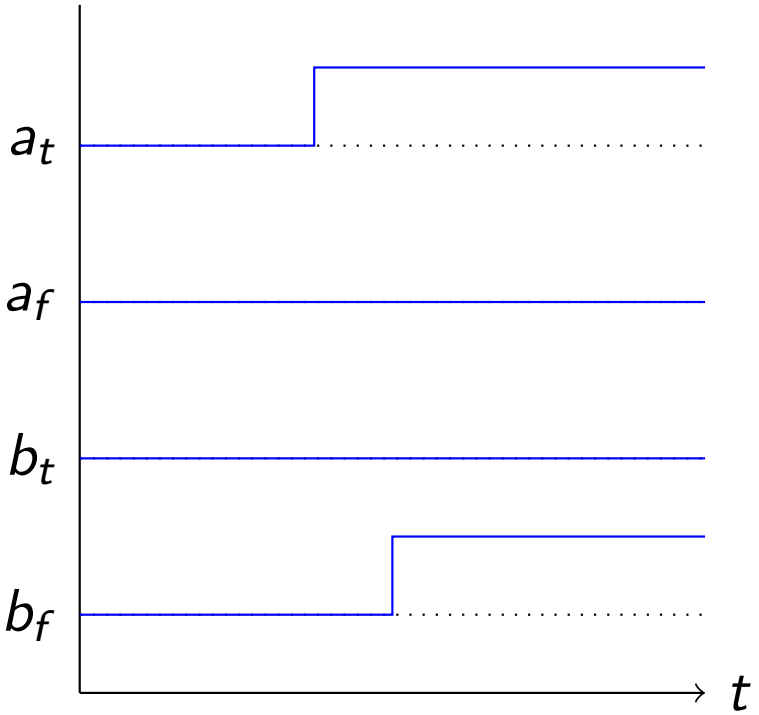
No glitches are possible.

$$[\![P]\!] \Vdash x \rightsquigarrow y$$
$$\preceq$$
$$x'$$

Interpretation of $\preceq$

$\preceq$ models the transition of signals from precharge state (NULL) to evaluation state (VALID).



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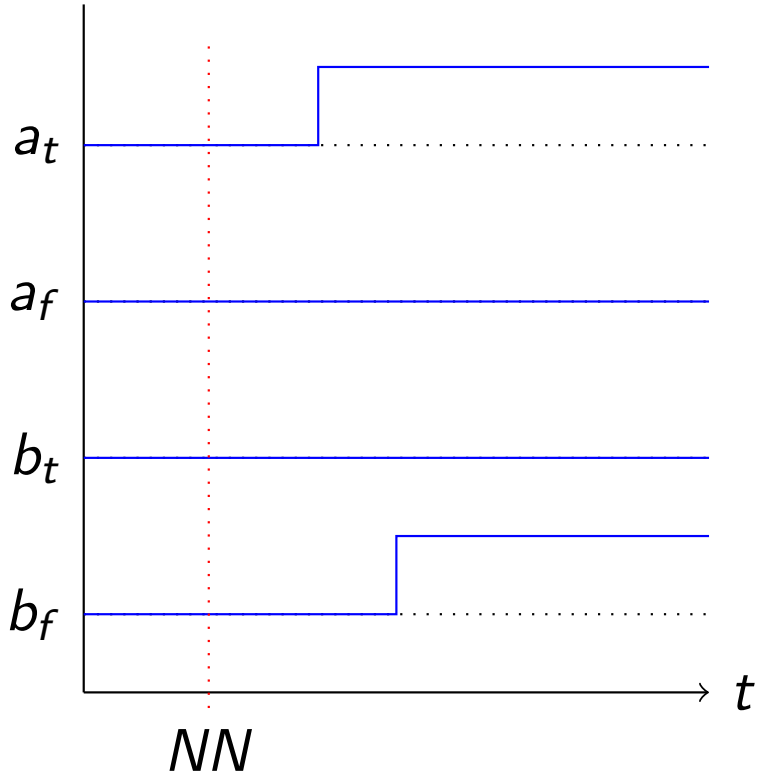

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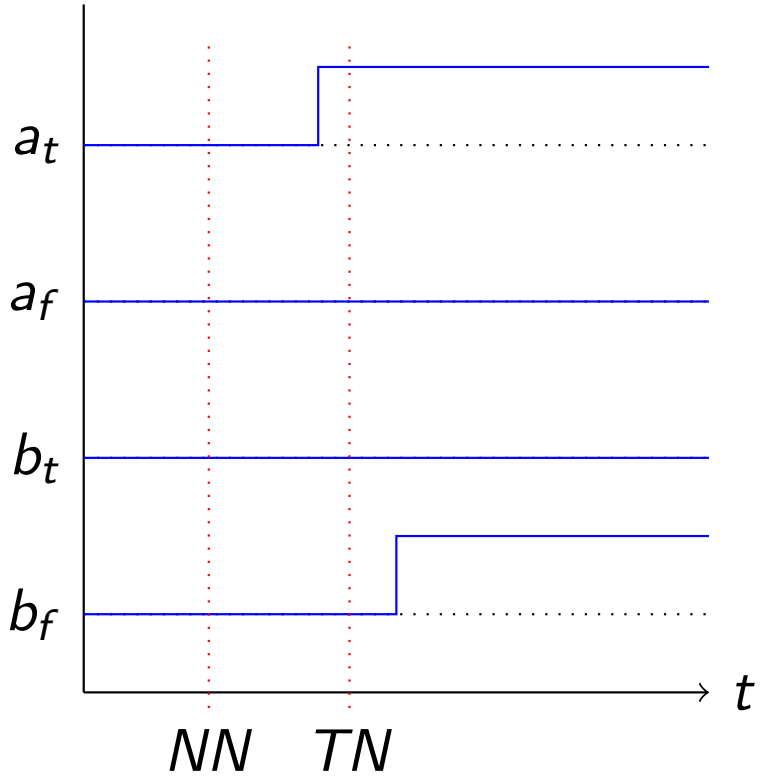

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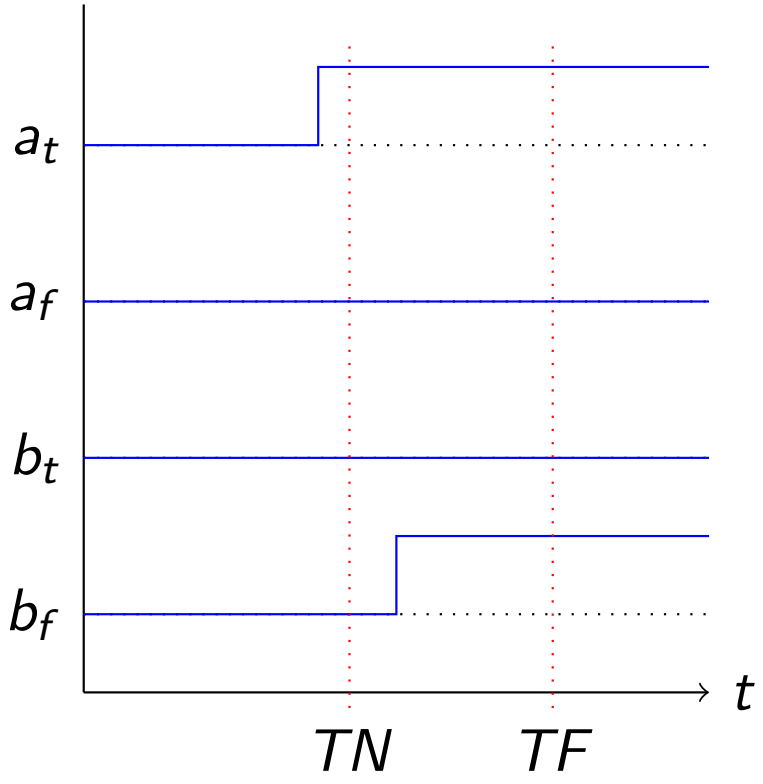

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The transformation is sound.

If $P \Vdash x \rightsquigarrow y$ then $[\![P]\!] \Vdash [x] \rightsquigarrow [y]$.

No glitches are possible.

$$\begin{array}{c} [\![P]\!] \Vdash x \rightsquigarrow y \\ \preceq \\ x' \end{array}$$

Properties

$[\![P]\!]$ fulfils the DPL invariants.

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$$\begin{array}{c} [\![P]\!] \Vdash x \rightsquigarrow y \\ \preceq \\ [\![P]\!] \Vdash x' \rightsquigarrow y' \end{array}$$

Properties

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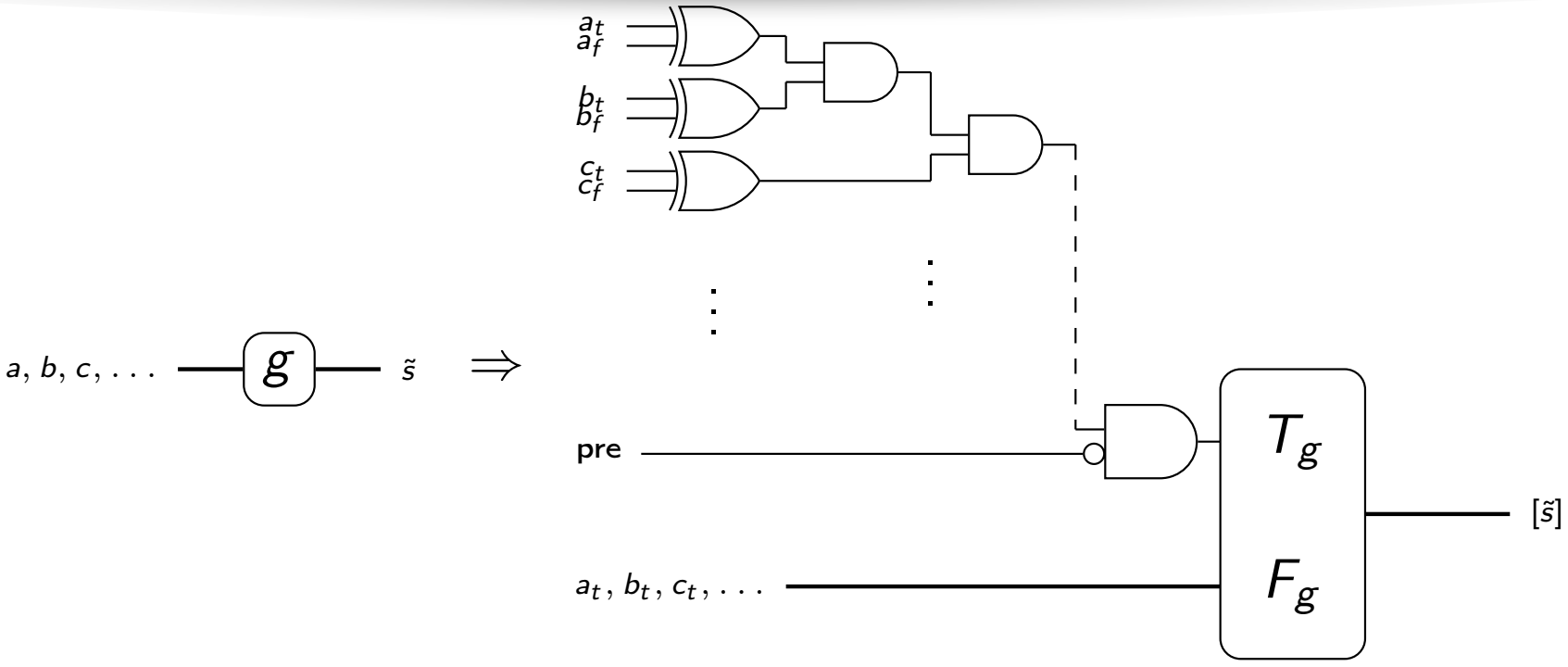
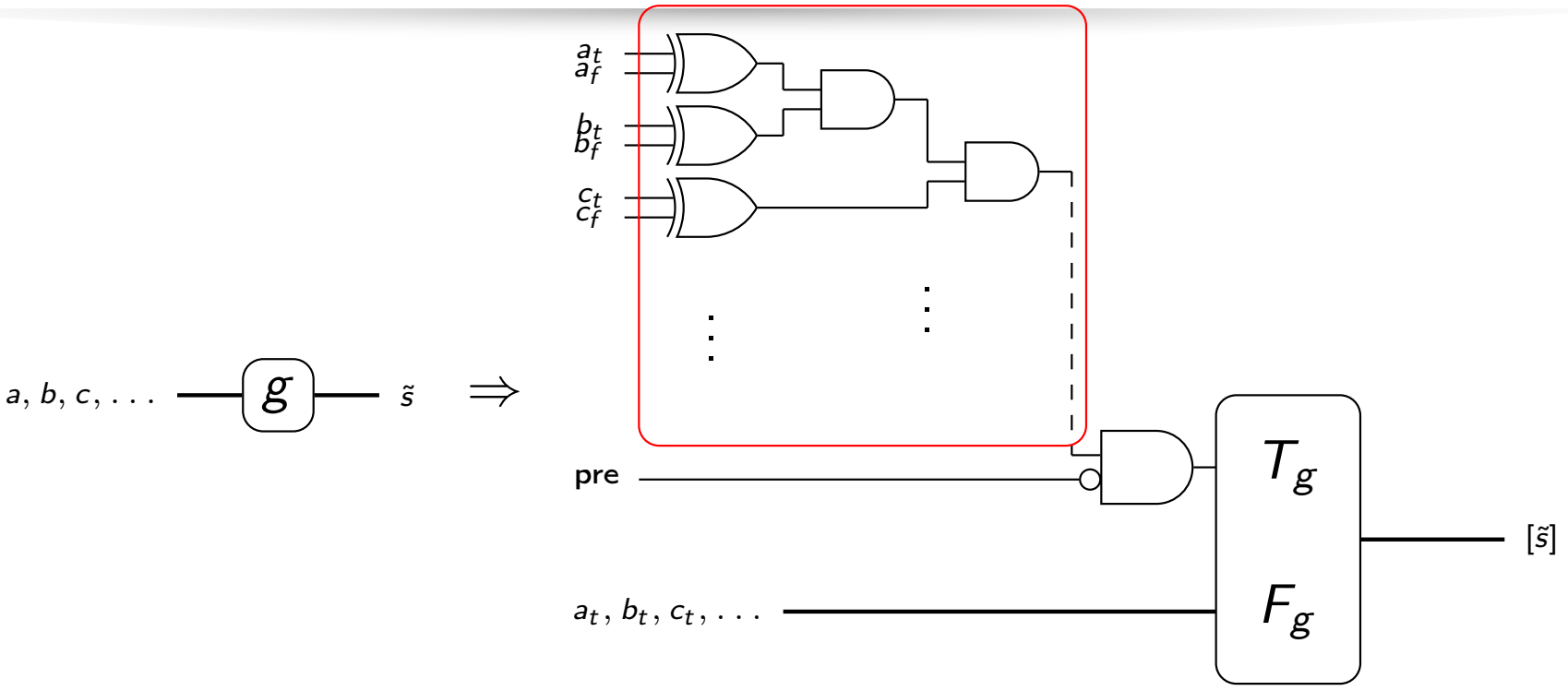
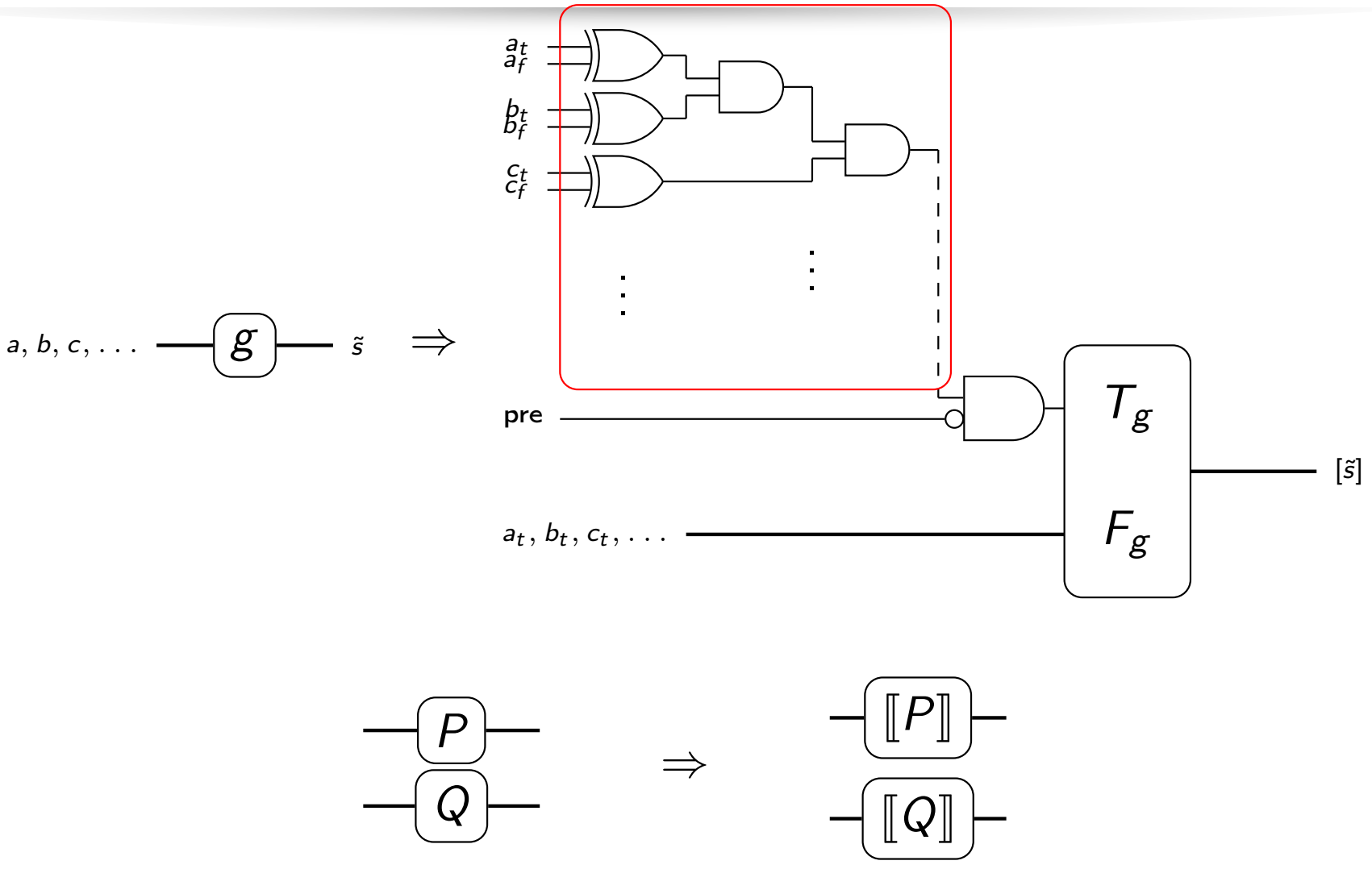
Transformation process



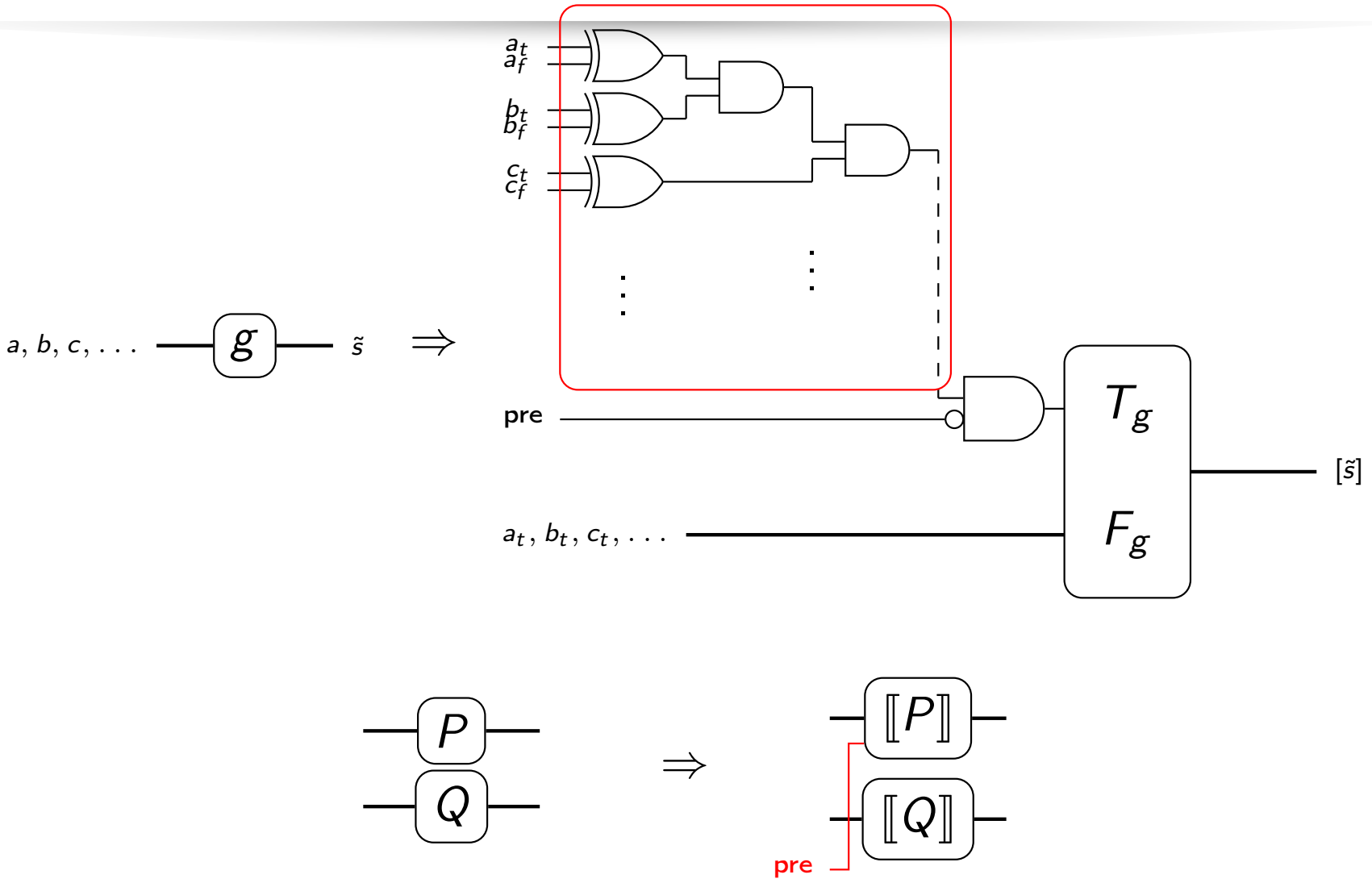
Transformation process



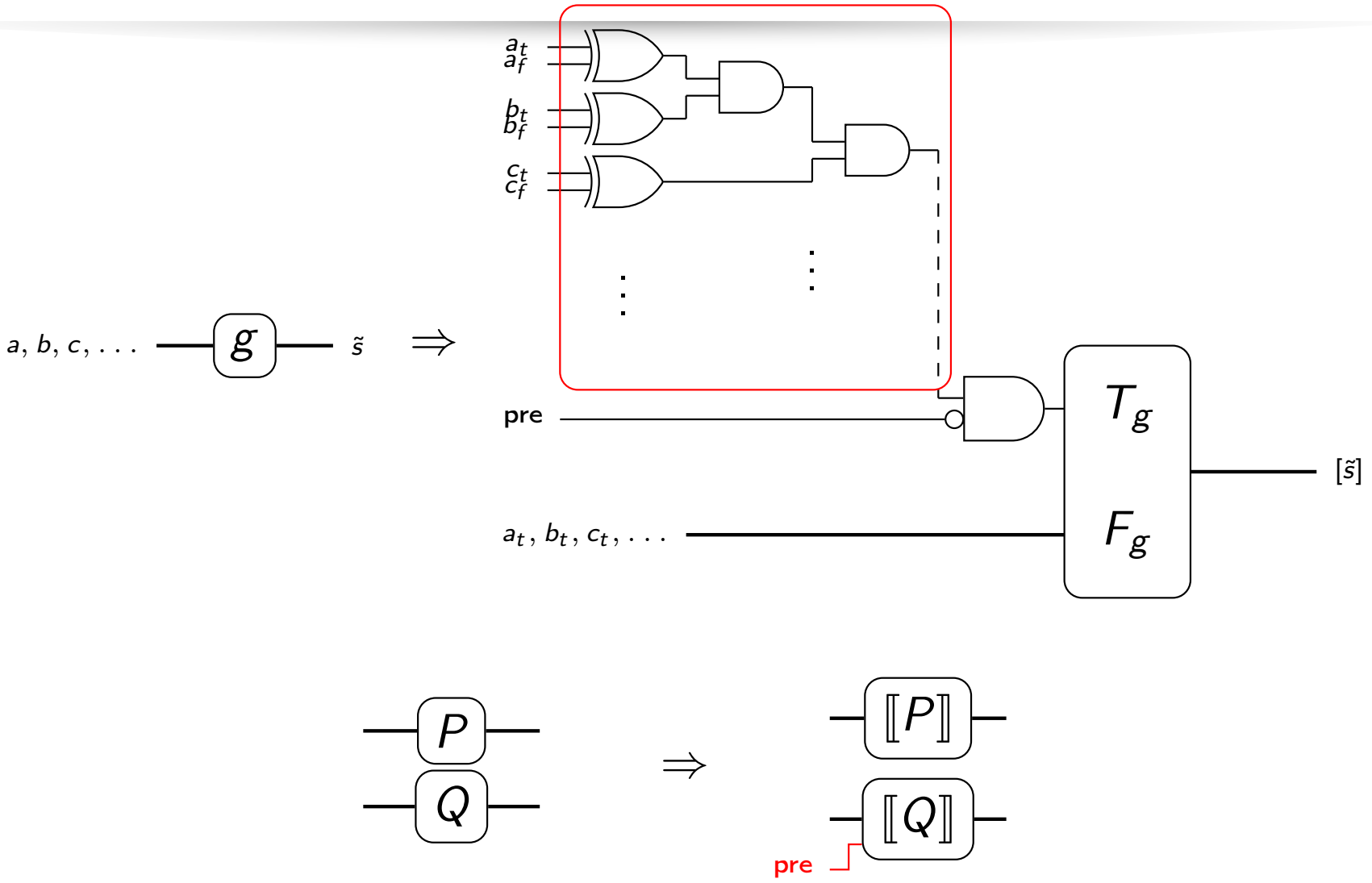
Transformation process



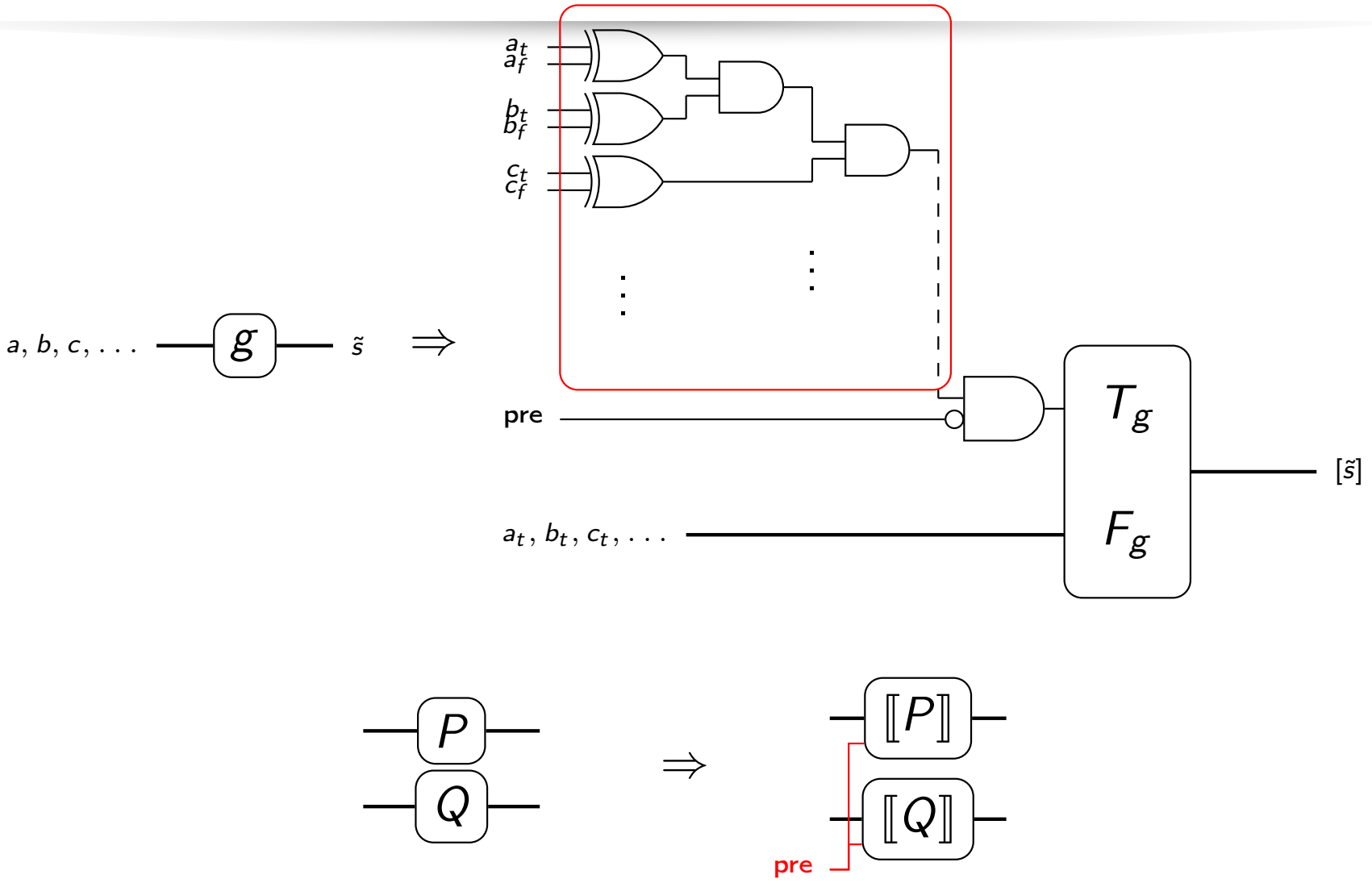
Transformation process



Transformation process



Transformation process



Properties

$[\![P]\!]$ fulfils the DPL invariants.

- If $[\![g]\!] \Vdash 1x \rightsquigarrow y$ then $y \in \mathrm{NULL}^*$.
- If $[\![P]\!] \Vdash \hat{1}x \rightsquigarrow y$ and $x \in \mathrm{NULL}^*$ then $y \in \mathrm{NULL}^*$.
- If $[\![P]\!] \Vdash \hat{0}x \rightsquigarrow y$ and $x \in \mathrm{VALID}^*$ then $y \in \mathrm{VALID}^*$.

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If $P \Vdash x \rightsquigarrow y$ then $[\![P]\!] \Vdash \hat{0}[x] \rightsquigarrow [y]$.

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The transformation is sound.

If $P \Vdash x \rightsquigarrow y$ then $[\![P]\!] \Vdash \hat{0}[x] \rightsquigarrow [y]$.

No glitches are possible.

If $[\![P]\!] \Vdash \hat{p}x \rightsquigarrow \hat{p}y$, $x \preceq x'$ and $[\![P]\!] \Vdash \hat{p}x' \rightsquigarrow \hat{p}y'$ then $y \preceq y'$.

Properties

There is no early-evaluation.

If $[\![P]\!] \Vdash \hat{0}x \rightsquigarrow y$ and $y \in \mathrm{VALID}^*$ then $x \in \mathrm{VALID}^*$.
(provided that P does not contain gates with 0 outputs)

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If $[\![P]\!] \Vdash \hat{0}x \rightsquigarrow y$ and $y \in \mathrm{VALID}^*$ then $x \in \mathrm{VALID}^*$.
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The transformation is complete.

If $[\![P]\!] \Vdash \hat{0}x' \rightsquigarrow y'$ and $y' \in \mathrm{VALID}^*$ then
there exists x, y such that $x' = [x]$, $y' = [y]$ and $P \Vdash x \rightsquigarrow y$.
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The secured circuit behaves the same on equivalent inputs.

$$[\![P]\!] \Vdash \hat{p}x \rightsquigarrow y$$

Properties

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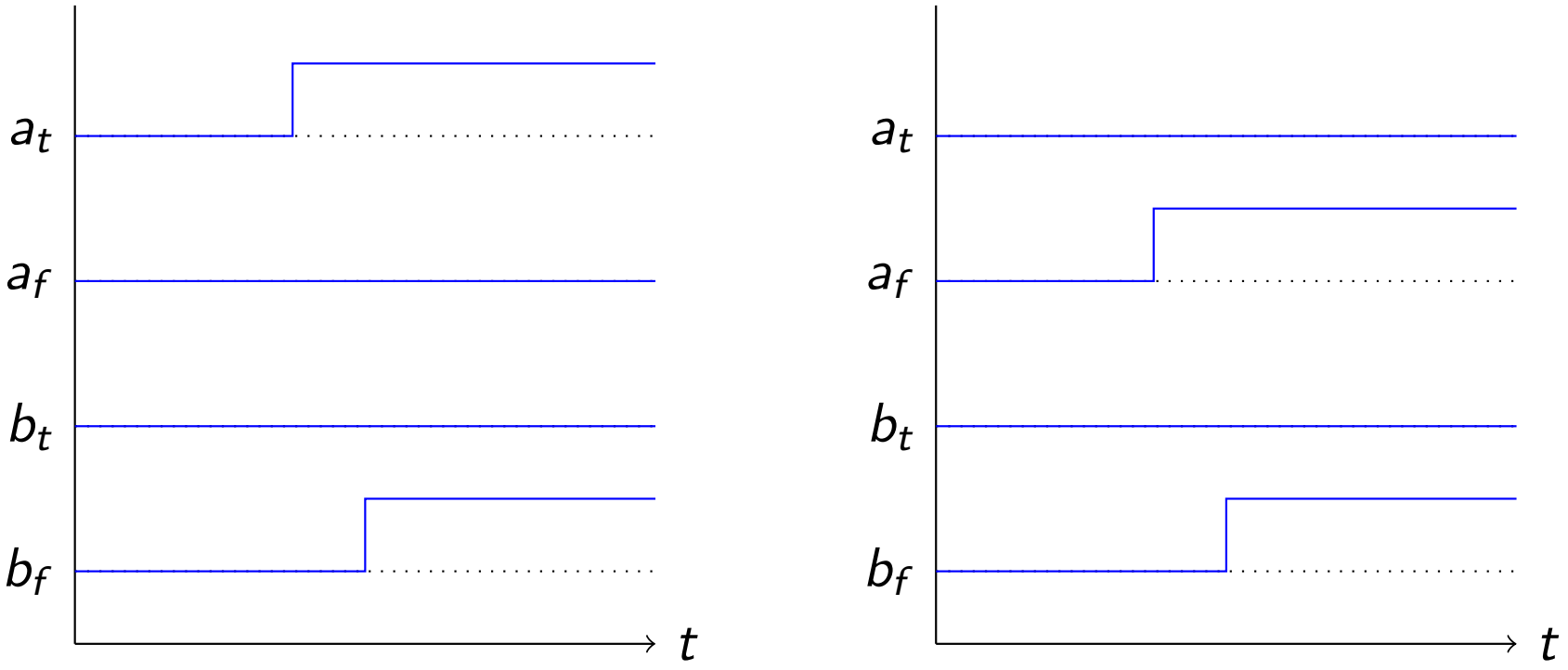
$$[\![P]\!] \Vdash \hat{p}x \rightsquigarrow y$$
$$\sim$$
$$\hat{p}x'$$

Interpretation of $\sim$

$\sim$ equates words which have the same amount of information, i.e. in which corresponding dual-rail signals have the same nature.



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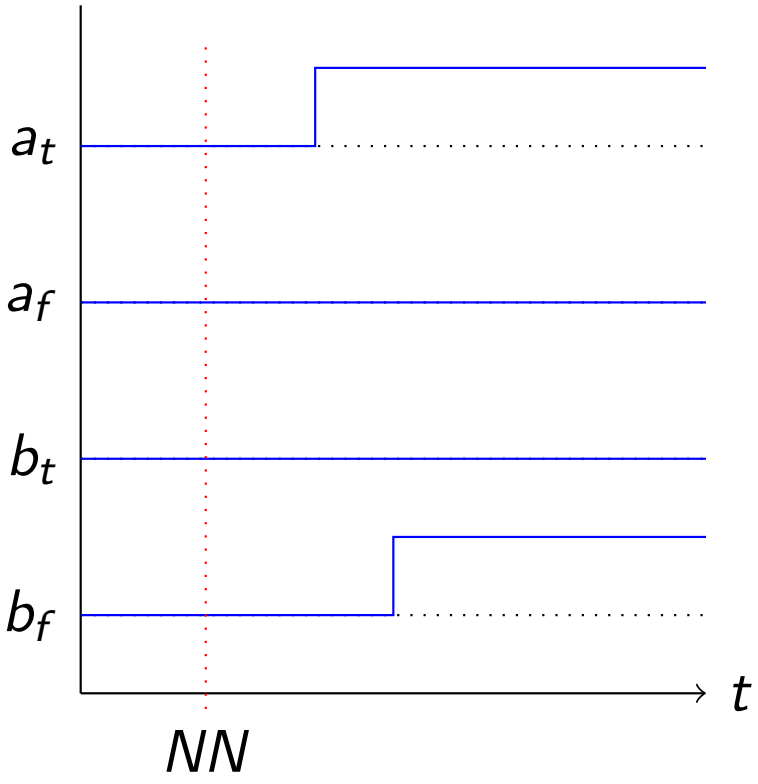

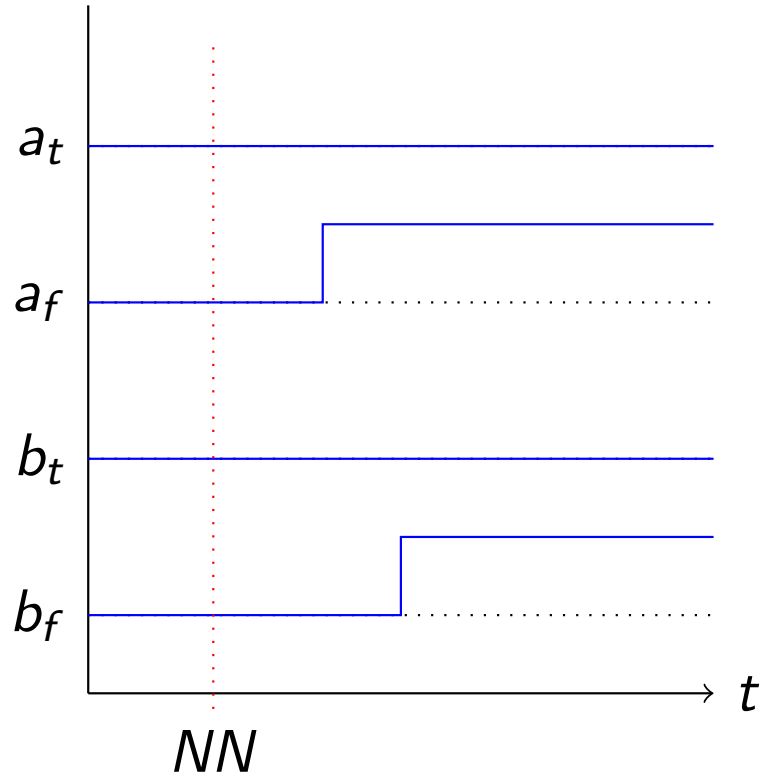

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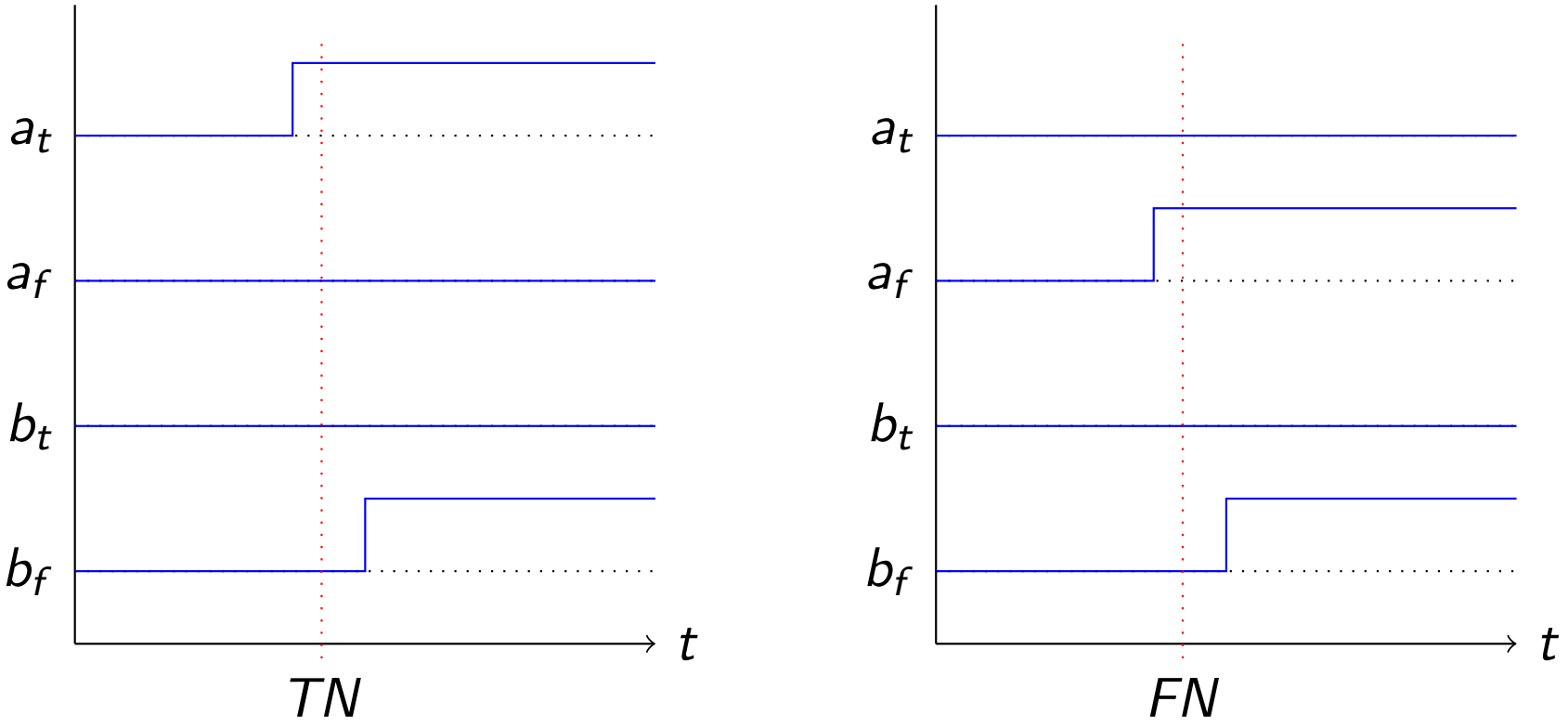

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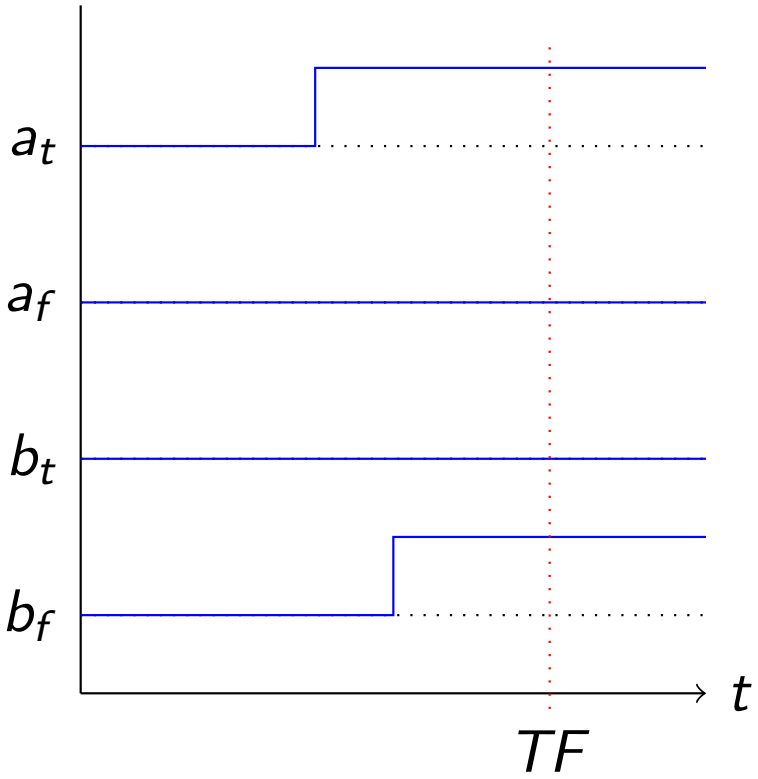

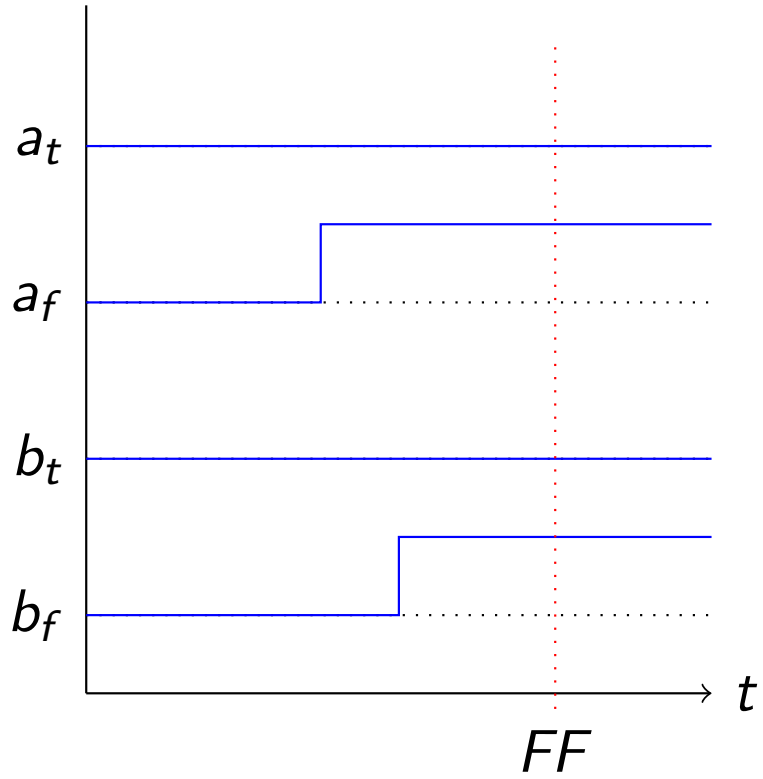

Properties

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If $[\![P]\!] \Vdash \hat{0}x \rightsquigarrow y$ and $y \in \mathrm{VALID}^*$ then $x \in \mathrm{VALID}^*$.
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The transformation is complete.

If $[\![P]\!] \Vdash \hat{0}x' \rightsquigarrow y'$ and $y' \in \mathrm{VALID}^*$ then
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The secured circuit behaves the same on equivalent inputs.

$$[\![P]\!] \Vdash \hat{p}x \rightsquigarrow y$$
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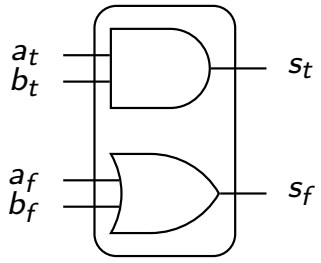
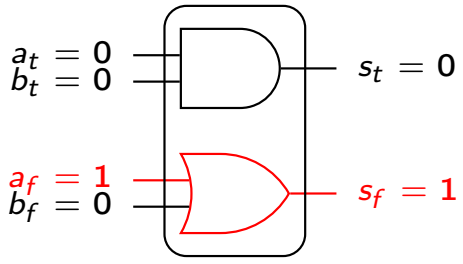
$$\begin{array}{ccc} [\![P]\!] \Vdash \hat{p}x & \rightsquigarrow & y \\ \sim & & \sim \\ [\![P]\!] \Vdash \hat{p}x' & \rightsquigarrow & y' \end{array}$$

Back to WDDL



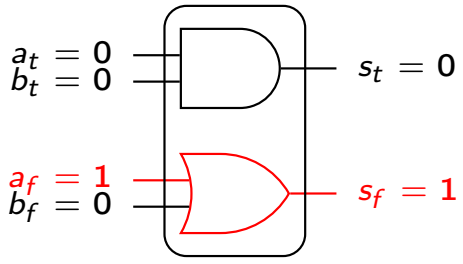
Back to WDDL



The $\mathrm{AND}_{\mathrm{WDDL}}$ gate suffers from early-evaluation.

$x = 0100 \notin \mathrm{VALID}^*$ and $y = 01 \in \mathrm{VALID}^*$

Back to WDDL



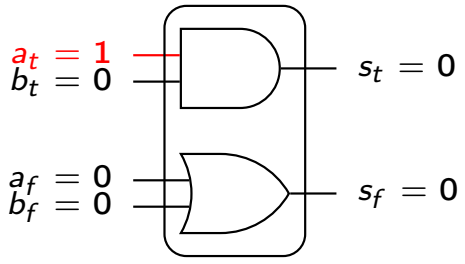
The $\mathrm{AND}_{\mathrm{WDDL}}$ gate suffers from early-evaluation.

$x = 0100 \notin \mathrm{VALID}^*$ and $y = 01 \in \mathrm{VALID}^*$

The $\mathrm{AND}_{\mathrm{WDDL}}$ gate behaves differently on equivalent inputs.

$x = 0100$ and $y = 01$

Back to WDDL



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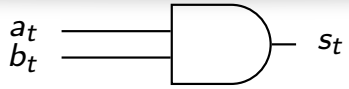
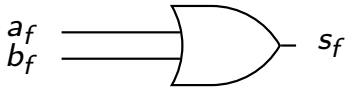
$x = 0100 \notin \mathrm{VALID}^*$ and $y = 01 \in \mathrm{VALID}^*$

The $\mathrm{AND}_{\mathrm{WDDL}}$ gate behaves differently on equivalent inputs.

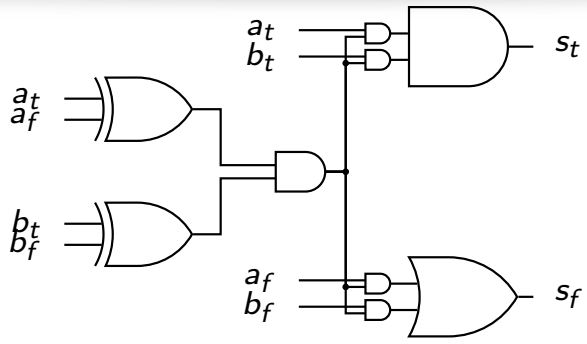
$x = 0100 \sim x' = 1000$ and $y = 01 \nsim y' = 00$

Discussion



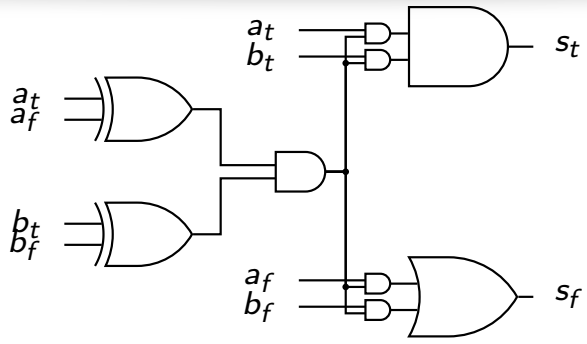


Discussion



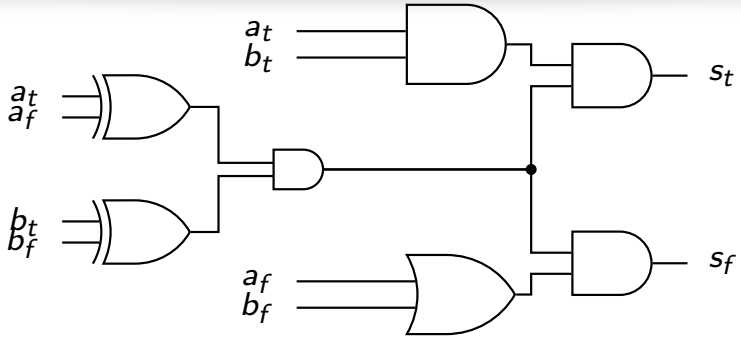
- BCDL fixes WDDL by adding a synchronisation barrier.

Discussion



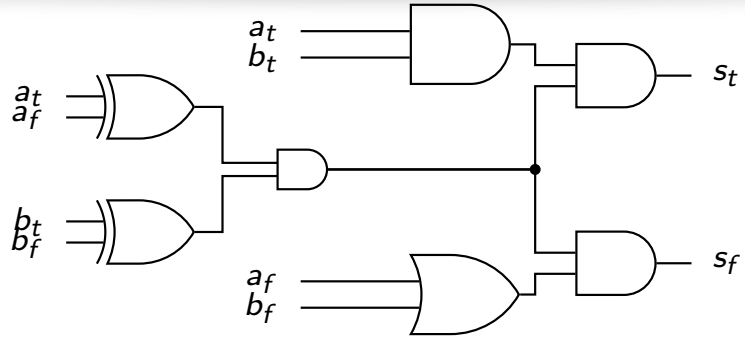
- BCDL fixes WDDL by adding a synchronisation barrier.
- How to address the race between the synchronisation signal and the data signals? (DRSL vulnerability)

Discussion



- BCDL fixes WDDL by adding a synchronisation barrier.
- How to address the race between the synchronisation signal and the data signals? (DRSL vulnerability)
- How to discriminate this circuit?

Discussion



- BCDL fixes WDDL by adding a synchronisation barrier.
- How to address the race between the synchronisation signal and the data signals? (DRSL vulnerability)
- How to discriminate this circuit?
  Measure the activity of circuits and show that the activity of a circuit is constant on equivalent inputs, i.e.

$$x \sim x' \Rightarrow \mu_C(x) = \mu_C(x')$$

Summary

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- We defined a calculus to describe combinational circuits.
- We defined formally WDDL and BCDL securisation process.
- We proved the correctness of these two transformations.
- Regarding security properties, we identified some necessary conditions to fulfil.

Perspectives

- Apply the model to other dual-rail styles.

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- Apply the model to other dual-rail styles.
- Refine the model.

The End

Thank You

Rotations

On words

- $\overrightarrow{\epsilon} = \epsilon$ and, for $a \in \Sigma, u \in \Sigma^*$, $\overrightarrow{ua} = au$
- $\overleftarrow{\epsilon} = \epsilon$ and, for $a \in \Sigma, u \in \Sigma^*$, $\overleftarrow{au} = ua$

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We define by induction on $n \in \mathbb{N}$ the circuit ror_n:

$$\begin{aligned}\mathrm{ror}_0 &:= \mathbf{0}\\ \mathrm{ror}_1 &:= \mathbf{I}\\ \mathrm{ror}_{n+2} &:= (\mathbf{I}^n \parallel \mathbf{X})\,;\,(\mathrm{ror}_{n+1} \parallel \mathbf{I})\end{aligned}$$

We have

$$\mathrm{ror}_n \Vdash x \rightsquigarrow y \iff |x| = n \wedge y = \overrightarrow{x}$$

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We define by induction on $n \in \mathbb{N}$ the circuit rol_n:

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We have

$$\mathrm{rol}_n \Vdash x \rightsquigarrow y \iff |x| = n \wedge y = \overleftarrow{x}$$

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We also have that:

- $\mathrm{ror}_n \,;\, \mathrm{rol}_n \equiv \mathsf{I}^n$
- $\mathrm{rol}_n \,;\, \mathrm{ror}_n \equiv \mathsf{I}^n$

Interleaving

On words

$\epsilon \,|||\, \epsilon := \epsilon$ and for $a, b \in \Sigma,\ u, v \in \Sigma^*,\ (au) \,|||\, (bv) := ab(u \,|||\, v)$

Interleaving

On words

$\epsilon \mid\mid\mid \epsilon := \epsilon$ and for $a, b \in \Sigma$, $u, v \in \Sigma^*$, $(au) \mid\mid\mid (bv) := ab(u \mid\mid\mid v)$

We define by induction on $n \in \mathbb{N}$ the circuit int_n:

$$\mathrm{int}_0 := \mathbf{0}$$
$$\mathrm{int}_{n+1} := (\mathbf{I} \| \mathrm{ror}_{n+1} \| \mathbf{I}^n) \,;\, (\mathbf{I} \| \mathbf{I} \| \mathrm{int}_n)$$

We have

$$\mathrm{int}_n \Vdash x \rightsquigarrow y \iff x = u \bullet v \wedge |u| = |v| = n \wedge y = u \mid\mid\mid v$$

Interleaving

On words

$\epsilon \mid\!\mid\!\mid \epsilon := \epsilon$ and for $a, b \in \Sigma$, $u, v \in \Sigma^*$, $(au) \mid\!\mid\!\mid (bv) := ab(u \mid\!\mid\!\mid v)$

We define by induction on $n \in \mathbb{N}$ the circuit unint_n:

$$\mathrm{unint}_0 := \mathbf{0}$$
$$\mathrm{unint}_{n+1} := (\mathbf{I} \| \mathbf{I} \| \mathrm{unint}_n) \,;\, (\mathbf{I} \| \mathrm{rol}_{n+1} \| \mathbf{I}^n)$$

We have

$$\mathrm{unint}_n \Vdash x \rightsquigarrow y \iff y = u \bullet v \wedge |u| = |v| = n \wedge x = u \mid\!\mid\!\mid v$$

Interleaving

On words

$\epsilon \,|||\, \epsilon := \epsilon$ and for $a, b \in \Sigma$, $u, v \in \Sigma^*$, $(au) \,|||\, (bv) := ab(u \,|||\, v)$

We also have that:

- $\mathrm{int}_n \,;\, \mathrm{unint}_n \equiv \mathsf{I}^{2n}$
- $\mathrm{unint}_n \,;\, \mathrm{int}_n \equiv \mathsf{I}^{2n}$